西安电子科技大学 微电之光 暑期学校

硬件工程师的摇篮

2025

EDA

7 17-22 HDL MCU

7 24-29

7 31-8 5 UVM FPGA

8 7-8 11 14nm /22nm VLSI

MCU FPGA

1 30%

2 40%

3 FPGA 15%

4 15%

8 12

8 13

221

14:30~14:50 /

14:50~15:00

15:00~15:15 PPT +

15:15~15:30

15:30~15:40 Intel

2017 6 15

Intel

(Cadence)

Synopsys

4

(2017 7 17-8 13)

+

9:00 12:00

14:30 17:30 19:00 22:00

EDA

1. Verilog HDL

2. Reuse Methodology Manual for System-on-a-Chip Designs KLUWER ACADEMIC Publishers Michael Keating etc
3. A Practical Guide to Adopting the UVM, Cadence Corp Sharon Rosenberg, Kathleen Meade
4. Advanced_ASIC_Chip_Synthesis_-_Using_Synopsys_Design_Compiler,physical_compiler_and_Primetime KLUWER ACADEMIC Publishers Himanshu Bhatnagar
5. Design Compiler User Guider Synopsys Corp
6. Formality User Guider Synopsys Corp
7. Prime time User Guider Synopsys Corp
8. IC Compiler User Guider Synopsys Corp
9. SoC Encounter User Guider cadence Corp

IC EDA

EDA

HDL EDA

FPGA UVM

HDL ARC

(Synopsys)

Day 1 Verilog HDL

1

2

3

Day2 Verilog HDL Testbench

Day3 Verilog HDL

Day4 ARC ISA

Day5 ARC IO

Day6 OS

( )

Day 1

1

2 ARC MeraWare toolkit

Day 2 MQX OS

1 MQX

2 MQX

3 MQX

Day 3 ARC EM Starter Kit

1 EM Kit FPGA

2 UART

Day 4

1 EDA

2

3

4

Day 5 DC

1 Pre-synthesis processes

2 DC 同

Day 6

1 Constraining

2 Timing

3 Synthesis

UVM FPG

(Intel)

Day 1 SystemVerilog

1

2 SystemVerilog

3

4

Day 2 UVM

1

2

Day 3 UVM

1

2

3

4

Day 4 FPGA

1 FPGA

2 FPGA

3

4

Day 5 FPGA

1 FPGA

2 Chipscope/SignalStorm

3

4 PS AS JTAG

Day 6 FPGA

1 FPGA

2 FPGA

14nm/22nm VLSI

(cadence -)

Day 1

Day 2

1 Floorplan

2 PG

Day 3

1

2

3

4

Day 4 1

Day 5 2

Day 6

1 -